

ISA Bus Technical Summary

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1.0 ISA Overview

The Industry Standard Architecture, or ISA, bus originated in the early 1980s at an IBM development lab in Boca Raton, Florida. The original IBM Personal Computer introduced in 1981 included the 8-bit subset of the ISA bus. In 1984, IBM introduced the PC-AT which was the first full 16-bit implementation of the ISA bus.

The "AT bus", as IBM originally called it, was first documented in an IBM publication called the *PC-AT Technical Reference*. The Technical Reference included schematics and BIOS listings that made it easy for other companies like Compaq to produce IBM compatible clones. The companies producing IBM compatibles could not use the "AT bus" name however since IBM had protected it with a trademark. In response, the industry coined "ISA" as a new name for the bus that was eventually adopted by everyone including IBM.

Although the PC-AT Technical Reference included detailed schematics and BIOS listings, it did not include the rigorous timings, rules, and other requirements that would make it a good bus specification. As a result, the various implementations of ISA were not always compatible with each other. Over time various ISA bus specifications were produced in an attempt to alleviate the compatibility problems. But unfortunately these specifications did not always agree with each other, so no single specification for the ISA bus was ever developed.

2.0 ISA Documents

2.1 ISA Specifications

Several documents that include specifications for the ISA bus are as follows:

- EISA Specification, Version 3.12* - This document includes specifications for ISA as well as the "Extended Industry Standard Architecture" that defined a 32-bit extension to the ISA bus. At last check, this document could be ordered for a fee from [Global Engineering Services](#).
- IEEE Draft Standard P996* - This document describes the mechanical and electrical specifications for standard PC-style systems. At last check it could be ordered for a fee from IEEE at <http://standards.ieee.org>.
- PS/2 Technical Reference - AT Bus Systems* - This document from IBM includes signal definitions and timing diagrams for the ISA bus used in some of IBM's PS/2 line of computers. At last check it could be ordered for a fee from IBM at <http://www.ibmink.ibm.com>. Search IBM's PubCatalog for document number S85F-1646.

2.2 ISA Books

Two books that provide good descriptions of the ISA bus are:

- ISA & EISA Theory and Operation*, by Edward Solari. ([Annabooks](#)) (ISBN 0-929392-15-9)
- ISA System Architecture*, by Don Anderson and Tom Shanley ([MindShare](#)) (ISBN 0-201-40996-8)

3.0 ISA Signal Descriptions

SA19 to SA0
System Address bits 19:0 are used to address memory and I/O devices within the system. These signals may be used along with LA23 to LA17 to address up to 16 megabytes of memory. Only the lower 16 bits are used during I/O operations to address up to 64K I/O locations. SA19 is the most significant bit. SA0 is the least significant bit. These signals are gated on the system bus when BALE is high and are latched on the falling edge of BALE. They remain valid throughout a read or write command. These signals are normally driven by the system microprocessor or DMA controller, but may also be driven by a bus master on an ISA board that takes ownership of the bus.

LA23 to LA17
Unlatched Address bits 23:17 are used to address memory within the system. They are used along with SA19 to SA0 to address up to 16 megabytes of memory. These signals are valid when BALE is high. They are "unlatched" and do not stay valid for the entire bus cycle. Decodes of these signals should be latched on the falling edge of BALE.

AEN
Address Enable is used to degate the system microprocessor and other devices from the bus during DMA transfers. When this signal is active the system DMA controller has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles.

BALE
Buffered Address Latch Enable is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AEN, it indicates a valid microprocessor or DMA address.

CLK
System Clock is a freerunning clock typically in the 8MHz to 10MHz range, although its exact frequency is not guaranteed. It is used in some ISA board applications to allow synchronization with the system microprocessor.

SD15 to SD0
System Data serves as the data bus bits for devices on the ISA bus. SD15 is the most significant bit. SD0 is the least significant bits. SD7 to SD0 are used for transfer of data with 8-bit devices. SD15 to SD0 are used for transfer of data with 16-bit devices. 16-bit devices transferring data with 8-bit devices shall convert the transfer into two 8-bit cycles using SD7 to SD0.

-DACK0 to -DACK3 and -DACK5 to -DACK7
DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests on DRQ0 to DRQ3 and DRQ5 to DRQ7.

DRQ0 to DRQ3 and DRQ5 to DRQ7
DMA Requests are used by ISA boards to request service from the system DMA controller or to request ownership of the bus as a bus master device. These signals may be asserted asynchronously. The requesting device must hold the request signal active until the system board asserts the corresponding DACK signal.

-IO CH CK
I/O Channel Check signal may be activated by ISA boards to request than a non-maskable interrupt (NMI) be generated to the system microprocessor. It is driven active to indicate a uncorrectable error has been detected.

I/O CH RDY
I/O Channel Ready allow slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signals normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read or write command. The signal is release high when the device is ready to complete the cycle.

-IOR
I/O Read is driven by the owner of the bus and instructs the selected I/O device to drive read data onto the data bus.

-IOW
I/O Write is driven by the owner of the bus and instructs the selected I/O device to capture the write data on the data bus.

IRQ3 to IRQ7
Interrupt Requests are used to signal the system microprocessor that an ISA board requires attention. An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the request through its interrupt service routine. These signals are prioritized with IRQ9 to IRQ12 and IRQ14 to IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 to IRQ 7 have the lowest priority (IRQ7 is the lowest).

-SMEMR
System Memory Read instructs a selected memory device to drive data onto the data bus. It is active only when the memory decode is within the low 1 megabyte of memory space. SMEMR is derived from MEMR and a decode of the low 1 megabyte of memory.

-SMEMW
System Memory Write instructs a selected memory device to store the data currently on the data bus. It is active only when the memory decode is within the low 1 megabyte of memory space. SMEMW is derived from MEMW and a decode of the low 1 megabyte of memory.

-MEMR
Memory Read instructs a selected memory device to drive data onto the data bus. It is active on all memory read cycles.

-MEMW
Memory Write instructs a selected memory device to store the data currently on the data bus. It is active on all memory write cycles.

-REFRESH
Memory Refresh is driven low to indicate a memory refresh operation is in progress.

OSC
Oscillator is a clock with a 70ns period (14.31818 MHz). This signal is not synchronous with the system clock (CLK).

RESET DRV
Reset Drive is driven high to reset or initialize system logic upon power up or subsequent system reset.

TC
Terminal Count provides a pulse to signal a terminal count has been reached on a DMA channel operation.

-MASTER
Master is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command.

-MEM CS16
Memory Chip Select 16 is driven low by a memory slave device to indicate it is capable of performing a 16-bit memory data transfer. This signal is driven from a decode of the LA23 to LA17 address lines.

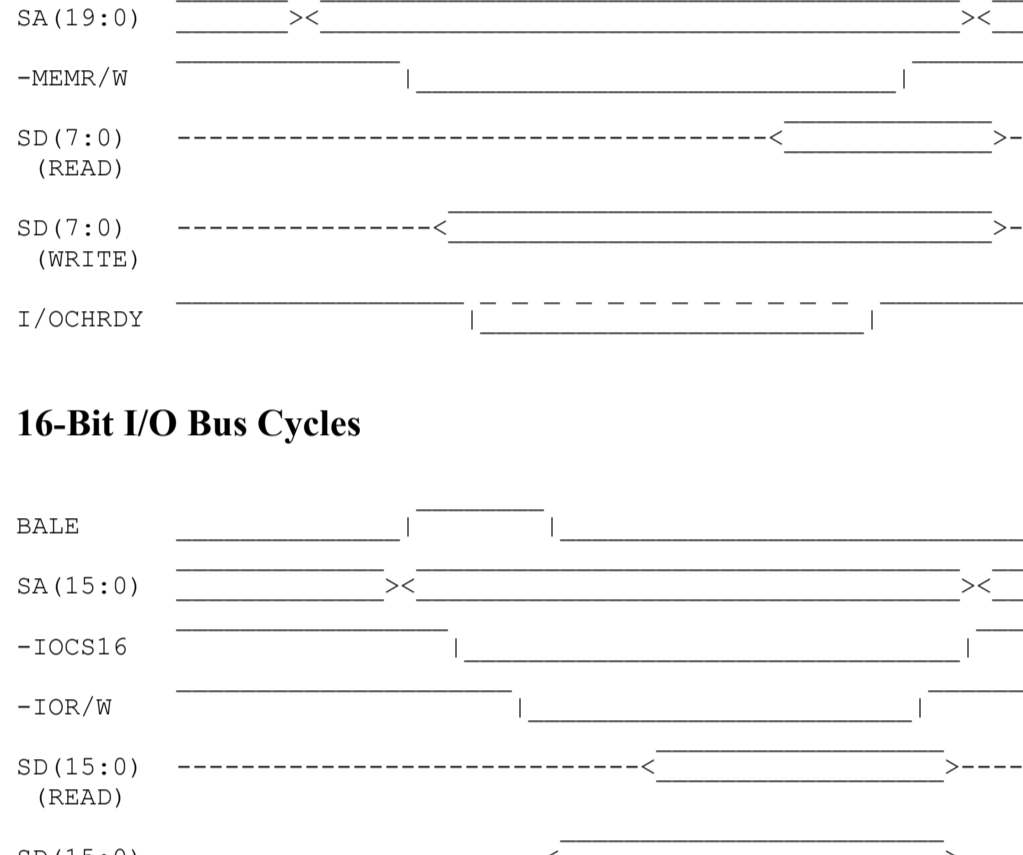
-IO CS16
I/O Chip Select 16 is driven low by a I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.

-OWS
Zero Wait State is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, -OWS is derived from an address decode.

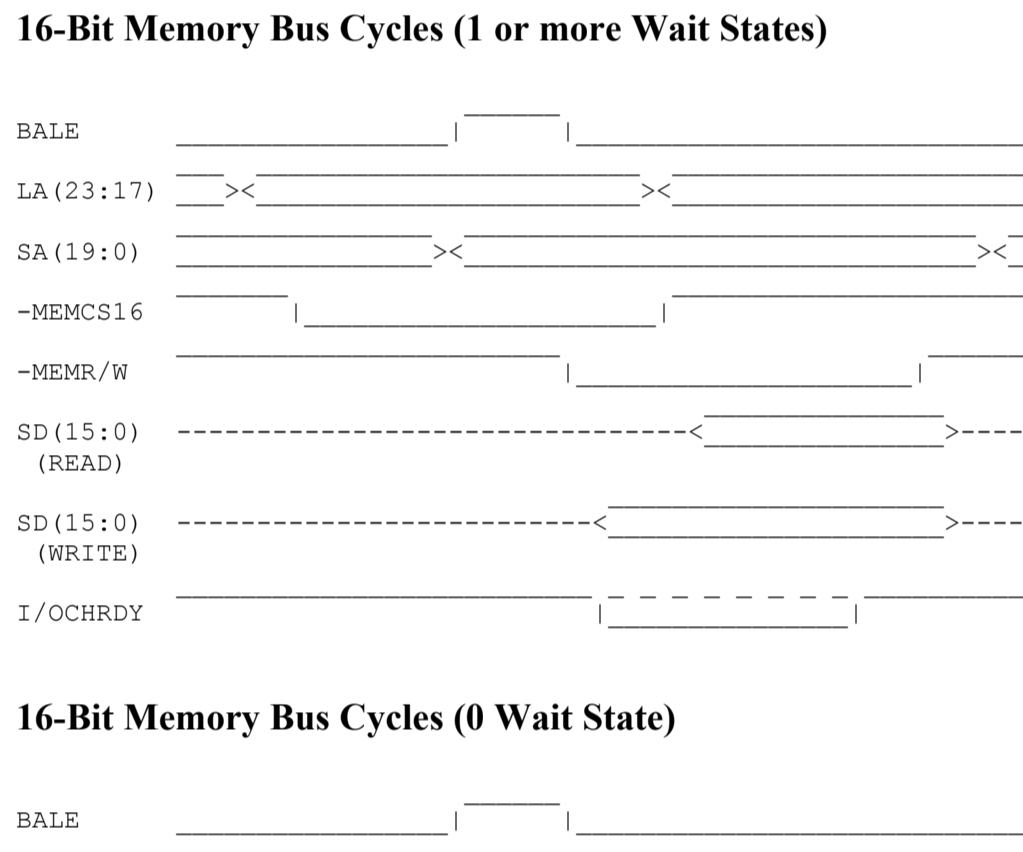
-SBHE
System Byte High Enable is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8).

4.0 ISA Bus Timing Diagrams

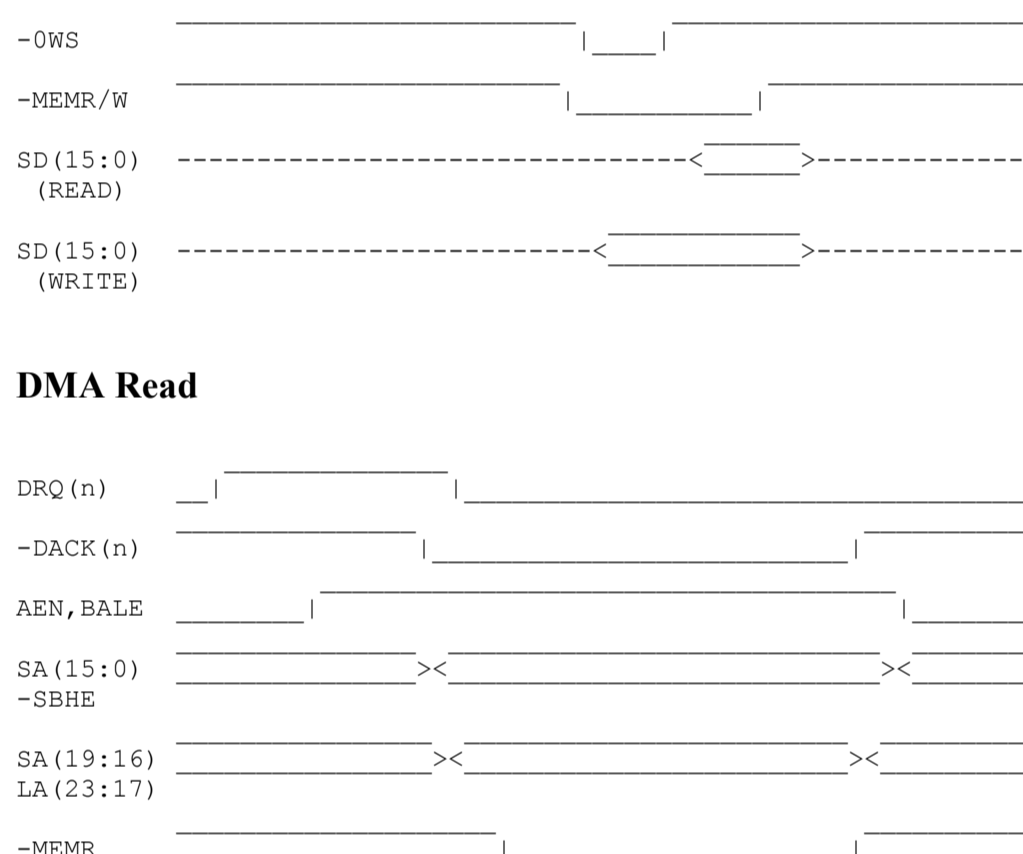
8-Bit I/O Bus Cycles



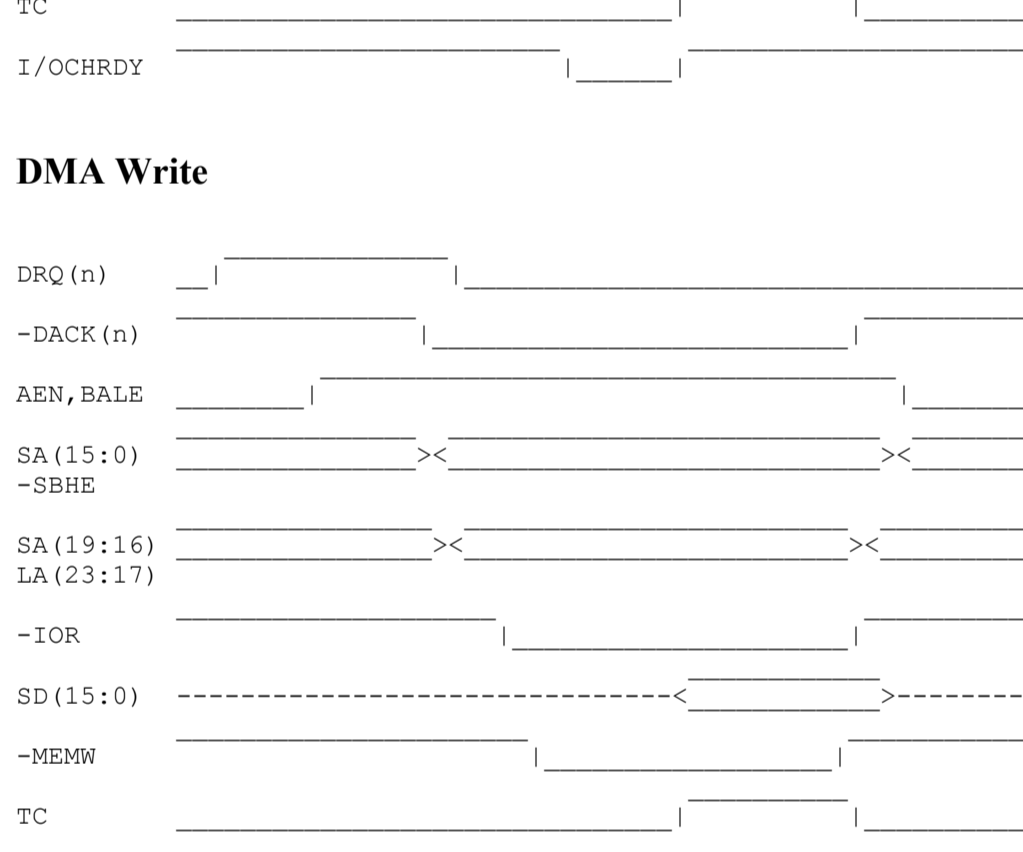
8-Bit Memory Bus Cycles



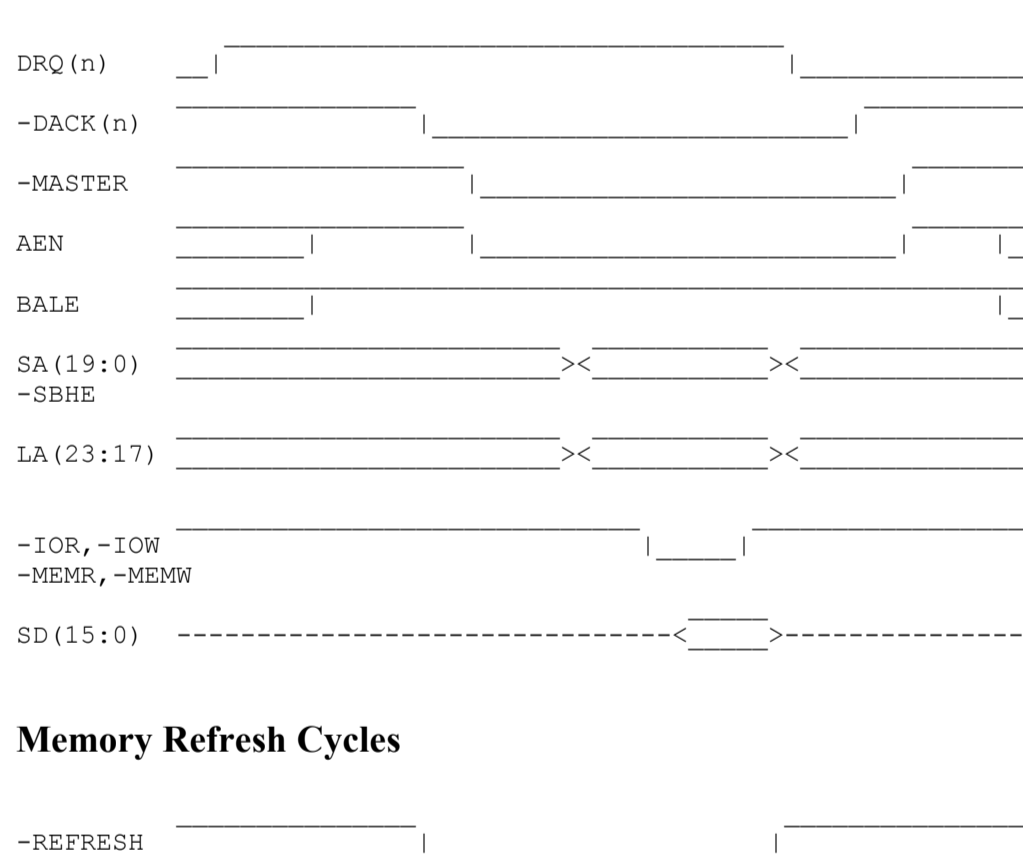
16-Bit I/O Bus Cycles



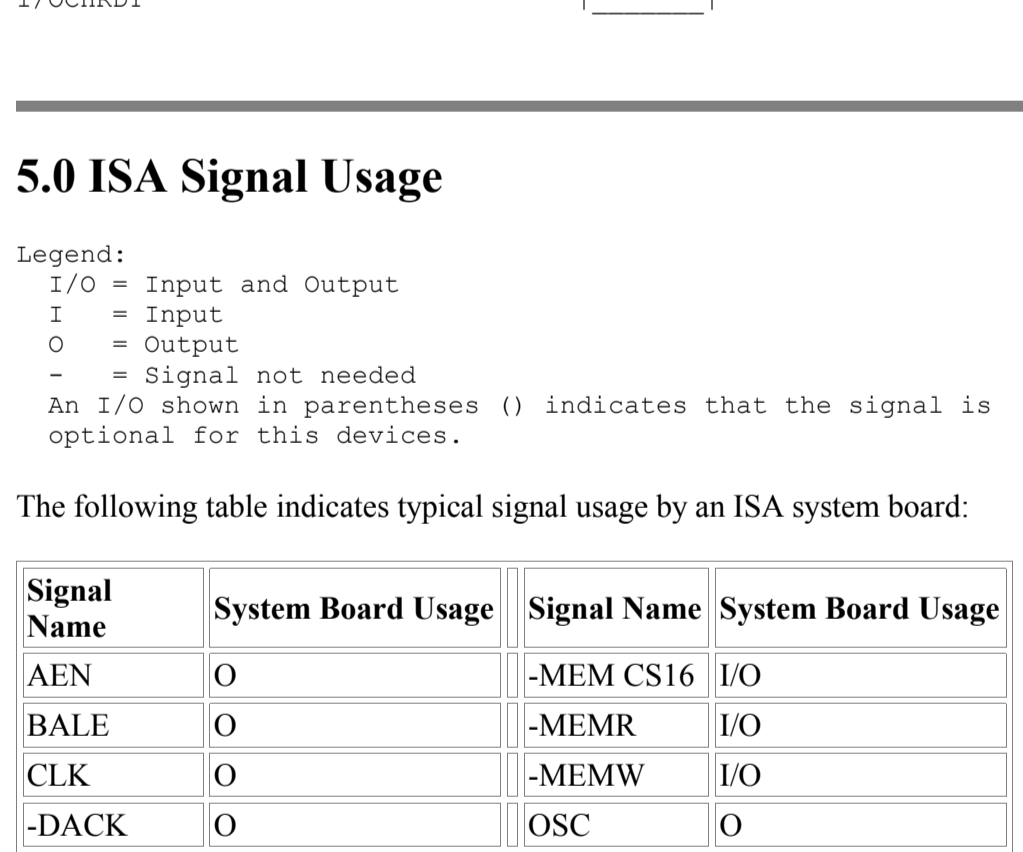
16-Bit Memory Bus Cycles (1 or more Wait States)



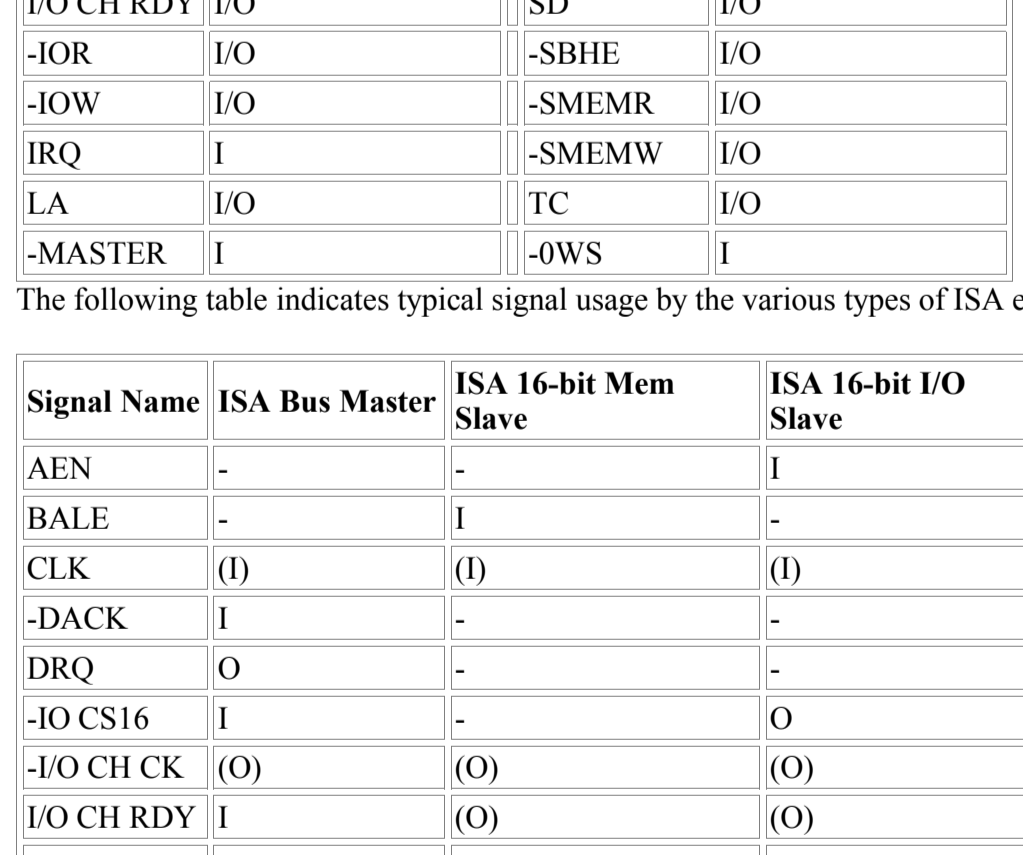
16-Bit Memory Bus Cycles (0 Wait State)



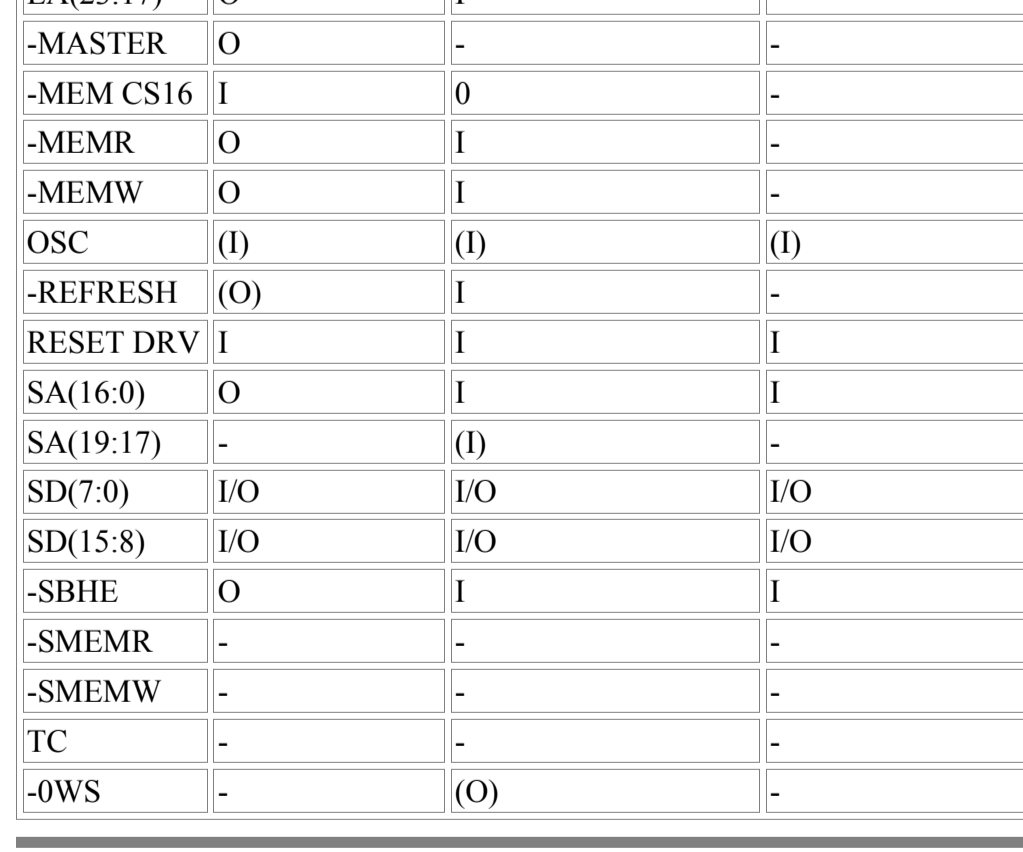
DMA Read



DMA Write



Alternate Bus Master Cycles



Memory Refresh Cycles



5.0 ISA Signal Usage

Legend:
 I/O = Input and Output
 I = Input
 O = Output
 - = Signal not needed
 An I/O shown in parentheses () indicates that the signal is optional for this devices.

The following table indicates typical signal usage by an ISA system board:

Signal Name	System Board Usage	Signal Name	System Board Usage
AEN	O	-MEM CS16	I/O
BALE	O	-MEMR	I/O
CLK	O	-MEMW	I/O
-DACK	O	OSC	O
DRQ	I	-REFRESH	I/O
-IO CS16	I	RESET DRV	O
-IO CH CK	I	SA	I/O
I/O CH RDY	I/O	SD	I/O
-IOR	I/O	-SBHE	I/O
-IOW	I/O	-SMEMR	I/O
IRQ	I	-SMEMW	I/O
LA	I/O	TC	I/O
-MASTER	I	-OWS	I

The following table indicates typical signal usage by the various types of ISA expansion boards:

Signal Name	ISA Bus Master	ISA 16-bit Mem Slave	ISA 16-bit I/O Slave	ISA 8-bit Mem Slave	ISA 8-bit I/O Slave	ISA DMA Device
AEN	-	-	I	-	I	-
BALE	-	I	-	(I)	-	-
CLK	(I)	(I)	(I)	(I)	(I)	(I)
-DACK	I	-	-	-	-	I
DRQ	O	-	-	-	-	O
-IO CS16	I	-	O	-	-	-
-IO CH CK	(O)	(O)	(O)	(O)	(O)	(O)
I/O CH RDY	I	(O)	(O)	(O)	(O)	-
-IOR	O	-	I	-	I	I
-IOW	O	-	I	-	I	I
IRQ	(O)	(O)	(O)	(O)	(O)	(O)
LA(23:17)	O	I	-	(I)	-	-
-MASTER	O	-	-	-	-	-
-MEM CS16	I	O	-	-	-	-
-MEMR	O	I	-	(I)	-	-
-MEMW	O	I	-	(I)	-	-
OSC	(I)	(I)	(I)	(I)	(I)	(I)
-REFRESH	(O)	I	-	I	-	-
RESET DRV	I	I	I	I	I	I
SA(16:0)	O	I	I	I	I	-
SA(19:17)	-	(I)	-	(I)	-	-
SD(7:0)	I/O	I/O	I/O	I/O	I/O	I/O
SD(15:8)	I/O	I/O	I/O	-	-	(I/O)
-SBHE	O	I	I	-	-	(I/O)
-SMEMR	-	-	-	I	-	-
-SMEMW	-	-	-	I	-	-
TC	-	-	-	-	-	(I)
-OWS	-	(O)	-	(O)	(O)	-

6.0 ISA Connector Pinout

Signal Name	Pin	Pin	Signal Name
Ground	B1	A1	-I/O CH CK
RESET DRV	B2	A2	SD7
+5 V dc	B3	A3	SD6
IRQ 9	B4	A4	SD5
-5 V dc	B5	A5	SD4
DRQ2	B6	A6	SD3
-12 V dc	B7	A7	SD2
-0WS	B8	A8	SD1
+12 V dc	B9	A9	SD0
Ground	B10	A10	I/O CH RDY
-SMEMW	B11	A11	AEN
-SMEMR	B12	A12	SA19
-IOW	B13	A13	SA18
-IOR	B14	A14	SA17
-DACK3	B15	A15	SA16
DRQ3	B16	A16	SA15
-DACK1	B17	A17	SA14
DRQ1	B18	A18	SA13
-REFRESH	B19	A19	SA12
CLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
-DACK2	B26	A26	SA5
TC	B27	A27	SA4
BALE	B28	A28	SA3
+5 V dc	B29	A29	SA2
OSC	B30	A30	SA1
Ground	B31	A31	SA0

Key

-MEM CS16	D1	C1	-SBHE
-IO CS16	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
-DACK0	D8	C8	LA17
DRQ0	D9	C9	-MEMR
-DACK5	D10	C10	-MEMW
DRQ5	D11	C11	SD08
-DACK6	D12	C12	SD09
DRQ6	D13	C13	SD10
-DACK7	D14	C14	SD11
DRQ7	D15	C15	SD12
+5 V dc	D16	C16	SD13
-MASTER	D17	C17	SD14
Ground	D18	C18	SD15